ANALOG DEVICES

Ultra-Low Bias Current Operational Amplifier

OP-80

FEATURES

- **Ultra-Low Bias Current:**
  - **150 femtoamps Typ .... at +25°C**
  - **300 femtoamps Typ .... at +85°C**
  - **500 femtoamps Typ .... at +125°C**
- **True Single Supply Operation**
  - **Common-Mode Range Includes Ground**
  - **Output Swings to Within 200μV of Ground Without Pulldown Resistors**
- **Low Supply Current .... 325μA Max**
- **Lower Cost Alternative to AD549 and OPA128**
- **Low Cost**
- **Inputs Protected Against 700V of Static Discharge**
- **Available in Die Form**

APPLICATIONS

- **Electrometer Amplifier Input Stage**
- **Photodiode and Infrared Detector Preamplifier**
- **Chemical and Gas Analyzers**
- **pH Probe Buffer Amplifier**
- **Fire Detectors**
- **High Voltage Voltmeters**
- **Charge Amplifiers**

GENERAL DESCRIPTION

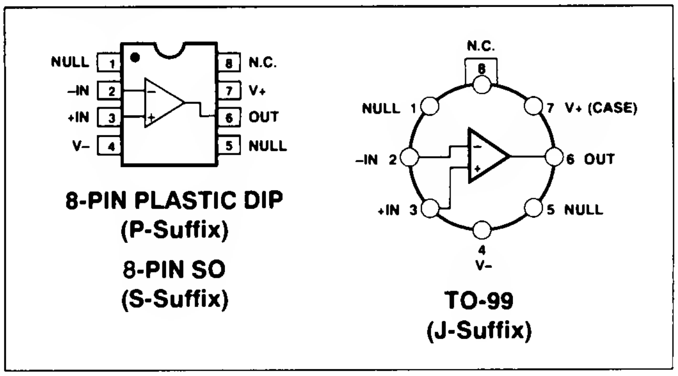
The OP-80 is a low cost CMOS operational amplifier offering exceptionally low input currents over a wide operating temperature range. Input current is typically 150 femtoamps at 25°C and increases to only 300 femtoamps at +85°C, with exceptionally high common-mode and differential input impedances. Incorporating a novel input protection design, the OP-80 achieves over 700V of ESD protection while maintaining very low input current.

For systems demanding both high performance at low supply voltages and high input impedances, the OP-80 is a powerful design tool. It is ideal for use in electrometers, portable medical instrumentation, chemical analyzers, smoke detectors, and sensitive current-to-voltage conversion circuits for photodiodes.

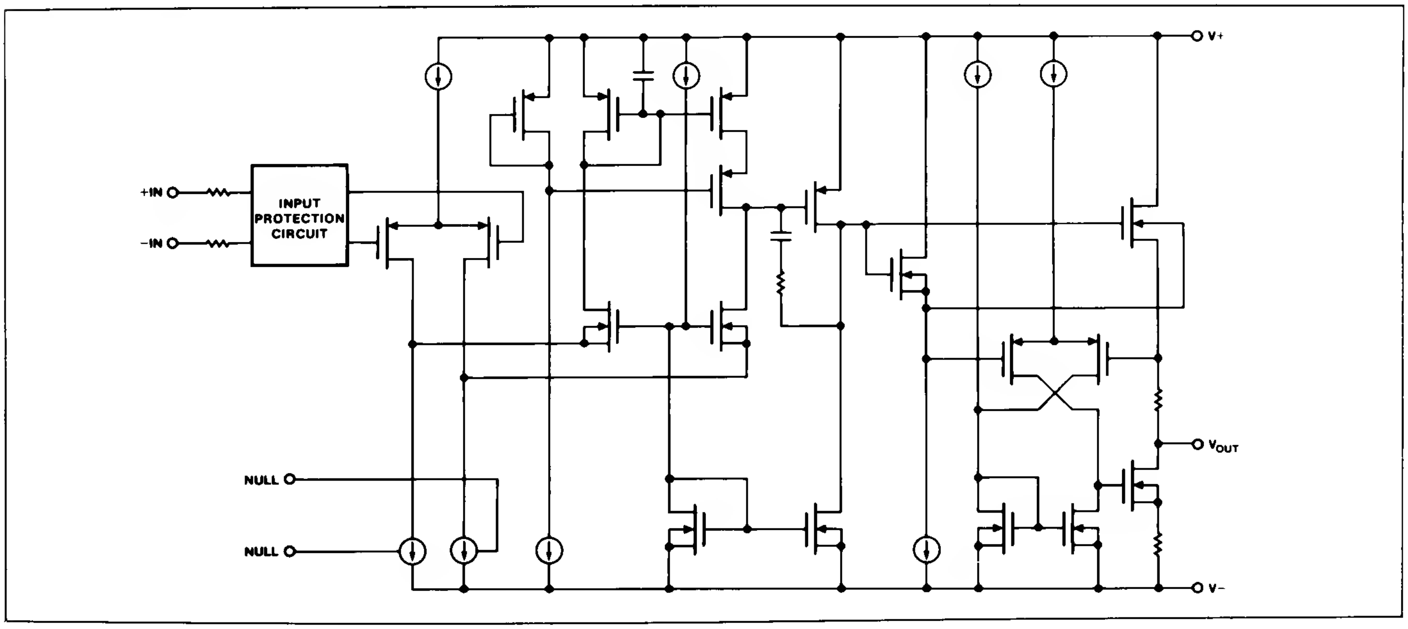
The low supply current minimizes thermal power dissipation, virtually eliminating the effects of chip self-heating. The OP-80's CMOS design gives a good speed/power ratio, permitting a

Continued

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC



GENERAL DESCRIPTION *Continued*

0.2V/µs minimum slew rate and a 300kHz gain-bandwidth product with unity-gain stability.

The OP-80 offers greater than 100dB of gain into a 2kΩ load, with output source/sink capability exceeding 15mA. In single supply applications, the OP-80's input range and output swing extends to ground. No pull-down resistor is required for the output to actively swing to within 200µV of ground.

Other applications for the OP-80 include precision pH, conductivity and ion measurement systems, low-level light and infrared detectors, barcode readers, and magnetic and electric field detectors. Its exceptional versatility makes it suitable for general-purpose applications, especially those requiring a single +5V supply.

The OP-80 conforms to the industry-standard 741 pinout, with the nulling potentiometer between pins 1 and 5, and the wiper to V–.

ORDERING INFORMATION †

I_B (pA)	PACKAGE TO-99	PACKAGE PLASTIC 8-PIN	OPERATING TEMPERATURE RANGE
2.0	OP80BJ*	–	MIL
0.250	OP80EJ	–	XIND
1.0	OP80FJ	–	XIND
2.0	–	OP80GP	XIND
2.0	–	OP80GS††	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages

†† For availability and burn-in information on SO packages, contact your local sales office.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage .... ±8V
Input Voltage (Note 2) .... +8V, –8.2V
Differential Input Voltage (Note 2) 16V
Output Short-Circuit Duration (Note 3) .... Indefinite
Operating Temperature Range
  OP-80G (P,S) .... –40°C to +85°C
  OP-80E,F,G (J) .... –40°C to +85°C
  OP-80B (J) .... –55°C to +125°C
Storage Temperature Range .... –65°C to +175°C
Junction Temperature Range .... –65°C to +175°C
Lead Temperature (Soldering, 10 sec) .... 300°C

PACKAGE TYPE	Θ_{jA} (Note 4)	Θ_{jC}	UNITS
TO-99 (J)	150	18	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W
8-Pin SO (S)	158	43	°C/W

NOTES:

1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. For supply voltages less than ±8V, the absolute maximum input voltage is equal to (V+) and (V– –0.2V).
3. The output may be shorted to ground indefinitely, but current must be externally limited to 25mA if the output is shorted to V+.
4. Θ_{jA} is specified for worst case mounting conditions, i.e., Θ_{jA} is specified for device in socket for TO and P-DIP packages; Θ_{jA} is specified for device soldered to printed circuit board for SO package.

ELECTRICAL CHARACTERISTICS at V_S = ±5V, V_{CM} = 0V, T_A = +25°C.

PARAMETER	SYMBOL	CONDITIONS	OP-80E MIN	OP-80E TYP	OP-80E MAX	OP-80F MIN	OP-80F TYP	OP-80F MAX	UNITS
Input Offset Voltage	V_{OS}		–	0.2	1.5	–	0.4	1.5	mV
Input Offset Current	I_{OS}		–	50	–	–	80	–	fA
Input Bias Current	I_B		–	0.15	0.250	–	0.2	1.0	pA
Input Voltage Range	IVR	Lower Limit Upper Limit	– –	(V –0V) (V + –1.5V)	– –	– –	(V –0V) (V + –1.5V)	– –	V
Common-Mode Rejection	CMR	V_{CM} = –4.75V, 3.5V	50	70	–	50	65	–	dB
Power-Supply Rejection	PSR	V_S = ±2.25V to ±8V	60	80	–	60	76	–	dB
Large-Signal Voltage Gain	A_{VO}	V_O = –4.5V to +3.25V, R_L = 10kΩ	100	400	–	100	300	–	V/mV

ELECTRICAL CHARACTERISTICS at $V_S = \pm5V$, $V_{CM} = 0V$, $T_A = +25°C$. *Continued*

PARAMETER	SYMBOL	CONDITIONS	OP-80E MIN	OP-80E TYP	OP-80E MAX	OP-80F MIN	OP-80F TYP	OP-80F MAX	UNITS
Output Voltage Swing	V_O	$V_S = \pm5V$, $R_L = 10k\Omega$	+3.5/ −4.75	+3.7/ −4.9	–	+3.5/ −4.75	+3.7/ −4.9	–	V
	V_{OH}	V+ = +5V, V− = 0V, $R_L = 10k\Omega$	+3.5	+3.7	–	+3.5	+3.7	–	V
	V_{OL}	V+ = +5V, V− = 0V, $R_L = 10k\Omega$	–	0.2	1	–	0.2	1	mV
Supply Current	I_{SY}	No Load	–	200	325	–	200	325	μA
Input Noise Voltage Density	e_n	$f_O = 1000Hz$	–	70	–	–	70	–	$nV/\sqrt{Hz}$
Output Current	I_{OUT}	Source Sink	25 15	45 24	– –	25 15	45 24	– –	mA
Slew Rate	SR	$A_V = +1$	0.2	0.4	–	0.2	0.4	–	V/μs
Gain-Bandwidth Product	GBW		–	300	–	–	300	–	kHz
Input Resistance		Common-Mode Differential	– –	10^{16} 10^{13}	– –	– –	10^{16} 10^{13}	– –	Ω

ELECTRICAL CHARACTERISTICS at $V_S = \pm5V$, $V_{CM} = 0V$, $T_A = +25°C$.

PARAMETER	SYMBOL	CONDITIONS	OP-80B MIN	OP-80B TYP	OP-80B MAX	UNITS
Input Offset Voltage	V_{OS}		–	0.5	2.0	mV
Input Offset Current	I_{OS}		–	100	–	fA
Input Bias Current	I_B		–	0.6	2.0	pA
Input Voltage Range	IVR	Lower Limit Upper Limit	– –	(V −0V) (V + −1.5V)	– –	V
Common-Mode Rejection	CMR	$V_{CM} = -4.75V, 3.5V$	50	65	–	dB
Power-Supply Rejection	PSR	$V_S = \pm2.25V$ to $\pm8V$	60	76	–	dB
Large-Signal Voltage Gain	A_{VO}	$V_O = -4.5V$ to $+3.25V$, $R_L = 10k\Omega$	100	225	–	V/mV
Output Voltage Swing	V_O	$V_S = \pm5V$, $R_L = 10k\Omega$	+3.5/ −4.75	+3.7/ −4.9	–	V
	V_{OH}	V+ = +5V, V− = 0V, $R_L = 10k\Omega$	+3.5	+3.7	–	V
	V_{OL}	V+ = +5V, V− = 0V, $R_L = 10k\Omega$	–	0.2	1	mV
Supply Current	I_{SY}	No Load	–	200	325	μA
Input Noise Voltage Density	e_n	$f_O = 1000Hz$	–	70	–	$nV/\sqrt{Hz}$
Output Current	I_{OUT}	Source Sink	25 15	45 24	– –	mA
Slew Rate	SR	$A_V = +1$	0.2	0.4	–	V/μs
Gain-Bandwidth Product		GBW	–	300	–	kHz
Input Resistance		Common-Mode Differential	– –	10^{16} 10^{13}	– –	Ω

ELECTRICAL CHARACTERISTICS at $V_S = \pm5V$, $V_{CM} = 0V$, $-40°C \le T_A \le +85°C$ for E/F grades; $-55°C \le T_A \le +125°C$ for B grade.

PARAMETER	SYMBOL	CONDITIONS	OP-80E/F MIN	OP-80E/F TYP	OP-80E/F MAX	OP-80B MIN	OP-80B TYP	OP-80B MAX	UNITS
Input Offset Voltage	V_{OS}		–	0.5	5.0	–	1.0	8.0	mV
Input Bias Current	I_B	(Note 1)	–	0.3	15	–	0.5	50	pA
Common-Mode Rejection	CMR	$V_{CM} = -4.75, 3.5V$	50	90	–	50	85	–	dB
Power-Supply Rejection	PSR	$V_S = \pm2.25V$ to $\pm8V$	60	85	–	57	80	–	dB
Large-Signal Voltage Gain	A_{VO}	$V_O = -4.5V$ to $+3.25V$, $R_L = 10k\Omega$	50	400	–	20	350	–	V/mV
Output Voltage Swing	V_O	$V_S = \pm5V$, $R_L = 10k\Omega$	+3.25/ –4.75	+3.7/ –4.9	–	+3.25/ –4.75	+3.7/ –4.9	–	V
	V_{OH}	$V+ = +5V$, $V- = 0V$, $R_L = 10k\Omega$	+3.25	+3.7	–	+3.25	+3.7	–	V
	V_{OL}	$V+ = +5V$, $V- = 0V$, $R_L = 10k\Omega$	–	0.1	1.0	–	0.15	1.0	mV
Supply Current	I_{SY}	No Load	–	275	400	–	275	400	µA
Output Current	I_{OUT}	Source	25	35	–	20	35	–	mA
		Sink	15	19	–	15	19	–	mA

NOTE:
1. Specification applies to +85°C and +125°C only.

ELECTRICAL CHARACTERISTICS at $V_S = \pm5V$, $V_{CM} = 0V$, $T_A = +25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-80G MIN	OP-80G TYP	OP-80G MAX	UNITS
Input Offset Voltage	V_{OS}		–	0.6	2.5	mV
Input Offset Current	I_{OS}		–	100	–	fA
Input Bias Current	I_B		–	400	2000	fA
Input Voltage Range	IVR	Lower Limit		(V– –0V)		V
		Upper Limit		(V+ –1.5V)		V
Common-Mode Rejection	CMR	$V_{CM} = -4.75V, 3.5V$	50	90	–	dB
Power-Supply Rejection	PSR	$V_S = \pm2.25V$ to $\pm8V$	60	80	–	dB
Large-Signal Voltage Gain	A_{VO}	$V_O = -4.5V$ to $+3.25V$, $R_L = 10k\Omega$	75	350	–	V/mV
Output Voltage Swing	V_O	$V_S = \pm5V$, $R_L = 10k\Omega$	+3.5/–4.75	+3.7/–4.9	–	V
	V_{OH}	$V+ = +5V$, $V- = 0V$, $R_L = 10k\Omega$	+3.5	+3.7	–	V
	V_{OL}	$V+ = +5V$, $V- = 0V$, $R_L = 10k\Omega$	–	0.2	1	mV

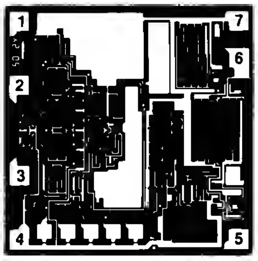
ELECTRICAL CHARACTERISTICS at $V_S = \pm5V$, $V_{CM} = 0V$, $T_A = +25°C$, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	OP-80G MIN	OP-80G TYP	OP-80G MAX	UNITS
Supply Current	I_{SY}	No Load	–	220	325	µA
Input Noise Voltage Density	e_n	$f_O = 1000Hz$	–	70	–	$nV/\sqrt{Hz}$
Output Current	I_{OUT}	Source	25	45	–	mA
		Sink	15	22	–	mA
Slew Rate	SR	$A_V = +1$	0.2	0.4	–	V/µs
Gain-Bandwidth Product	GBW		–	300	–	kHz
Input Resistance		Common-Mode	–	10^{16}	–	Ω
		Differential	–	10^{13}	–	Ω

ELECTRICAL CHARACTERISTICS at $V_S = \pm5V$, $V_{CM} = 0V$, $-40°C \le T_A \le +85°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-80G MIN	OP-80G TYP	OP-80G MAX	UNITS
Input Offset Voltage	V_{OS}		–	2.0	7.0	mV
Input Bias Current	I_B		–	0.6	50	pA
Common-Mode Rejection	CMR	$V_{CM} = -4.75V, 3.5V$	50	80	–	dB
Power-Supply Rejection	PSR	$V_S = \pm2.25V$ to $\pm8V$	57	80	–	dB
Large-Signal Voltage Gain	A_{VO}	$V_O = -4.5V$ to $+3.25V$, $R_L = 10k\Omega$	50	300	–	V/mV
Output Voltage Swing	V_O	$V_S = \pm5V$, $R_L = 10k\Omega$	+3.25/–4.50	+3.7/–4.9	–	V
	V_{OH}	$V+ = +5V$, $V- = 0V$, $R_L = 10k\Omega$	+3.25	+3.7	–	V
	V_{OL}	$V+ = +5V$, $V- = 0V$, $R_L = 10k\Omega$	–	0.2	1	mV
Supply Current	I_{SY}	No Load	–	275	400	µA
Output Current	I_{OUT}	Source	25	35	–	mA
		Sink	15	19	–	mA

DICE CHARACTERISTICS



DIE SIZE 0.070 X 0.069 inch, 4,830 sq. mils
(1.78 X 1.75mm, 3.12 sq. mm)

1. NULL
2. INPUT (–)
3. INPUT (+)
4. V–
5. NULL
6. OUTPUT
7. V+

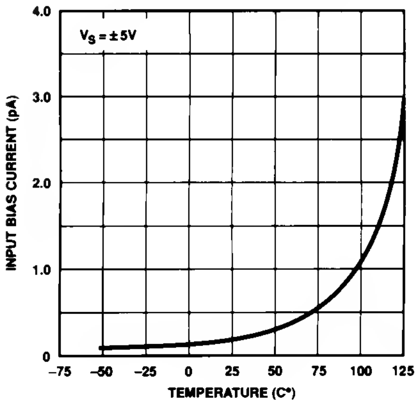
WAFER TEST LIMITS at $V_S = \pm 5V$, $V_{CM} = 0V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-80G LIMITS	UNITS
Input Offset Voltage	V_{OS}		2.5	mV MAX
Input Bias Current	I_B		50	pA MAX
Common-Mode Rejection	CMR	$V_{CM} = -4.75V, +3.5$	50	dB MIN
Power-Supply Rejection	PSR	$V_S = \pm 2.25V$ to $\pm 8V$	60	dB MIN
Large-Signal Voltage Gain	A_{VO}	$V_O = -4.5V$ to $+3.25V$ $R_L = 10k\Omega$	75	V/mV MIN
Output Voltage Swing	V_O	$V_S = \pm 5V$, $R_L = 10k\Omega$	+3.5/–4.75	V MIN
	V_{OH}	$V+ = +5V$, $V- = 0V$, $R_L = 10k\Omega$	+3.5	V MIN
	V_{OL}	$V+ = +5V$, $V- = 0V$, $R_L = 10k\Omega$	1	mV MAX
Supply Current	I_{SY}	No Load	325	µA MAX
Output Current	I_{OUT}	Source Sink	25 15	mA MIN

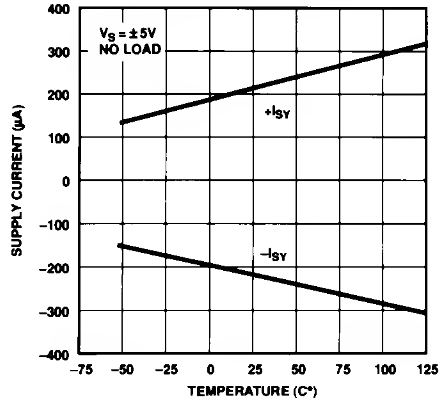
NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS

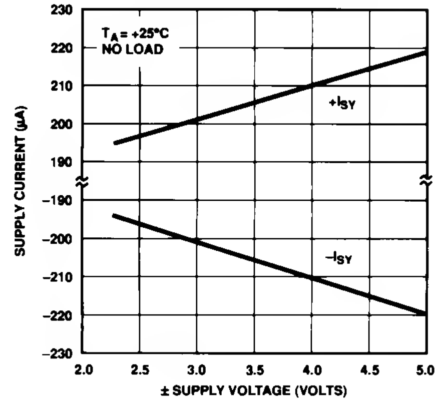
INPUT BIAS CURRENT vs TEMPERATURE



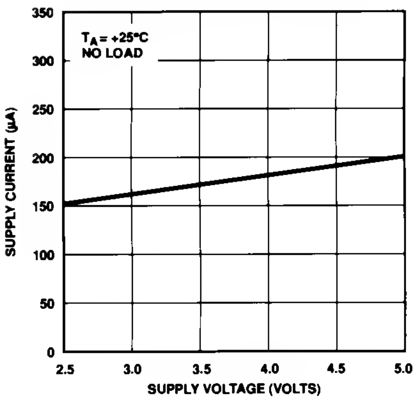
SUPPLY CURRENT vs TEMPERATURE



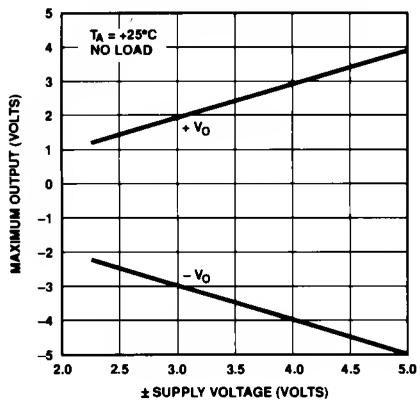
SUPPLY CURRENT vs SUPPLY VOLTAGE



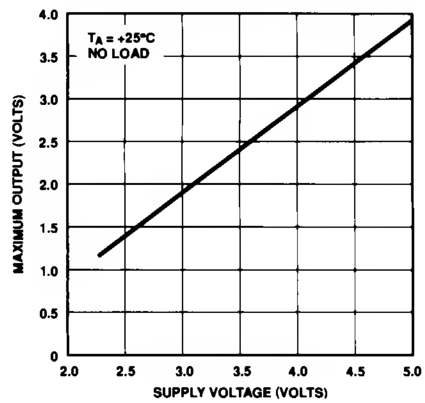
SUPPLY CURRENT vs SINGLE SUPPLY VOLTAGE



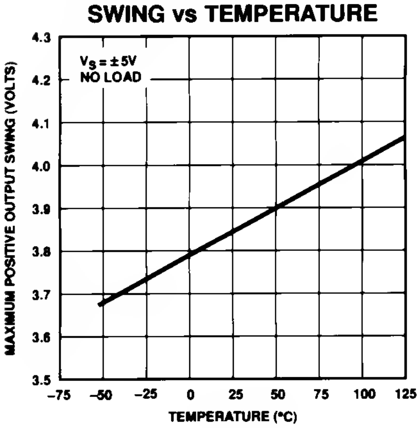
MAXIMUM OUTPUT VOLTAGE vs SUPPLY VOLTAGE



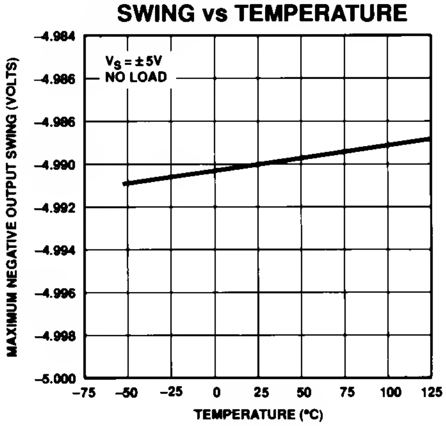
OUTPUT VOLTAGE SWING vs SINGLE SUPPLY VOLTAGE



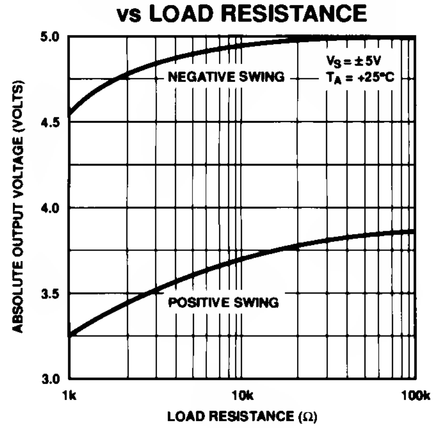
MAXIMUM POSITIVE OUTPUT SWING vs TEMPERATURE



MAXIMUM NEGATIVE OUTPUT SWING vs TEMPERATURE

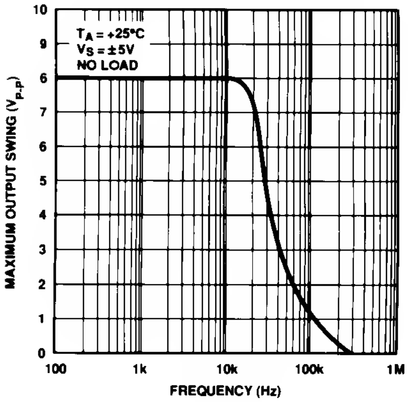


MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE

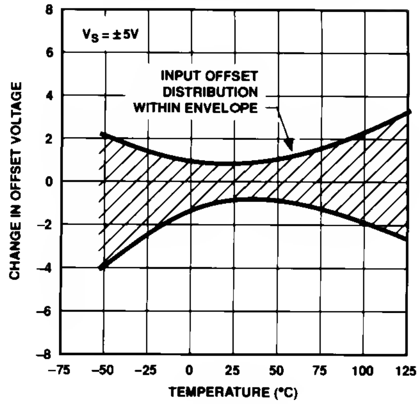


TYPICAL ELECTRICAL CHARACTERISTICS *Continued*

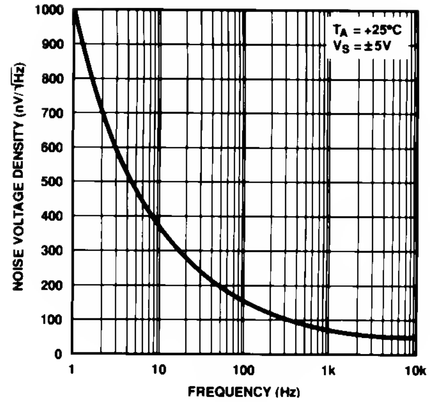
MAXIMUM OUTPUT SWING vs FREQUENCY



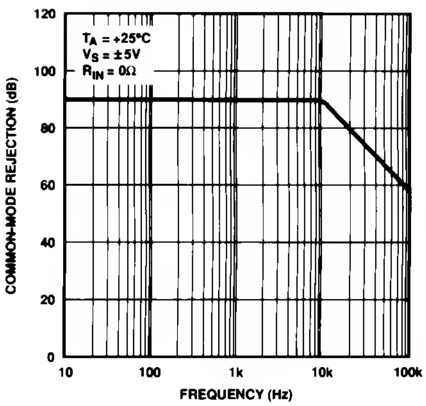
INPUT OFFSET VOLTAGE vs TEMPERATURE



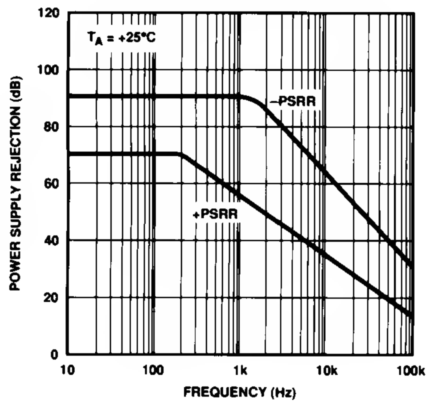
NOISE VOLTAGE DENSITY vs FREQUENCY



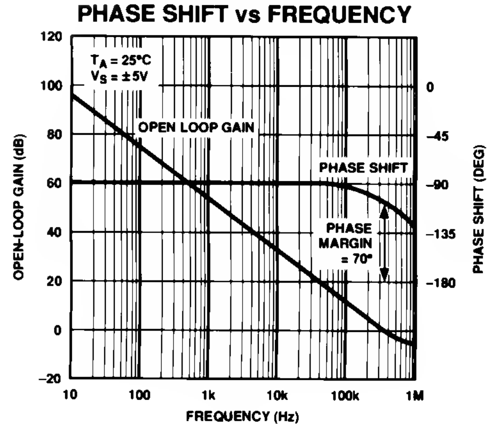
COMMON-MODE REJECTION vs FREQUENCY



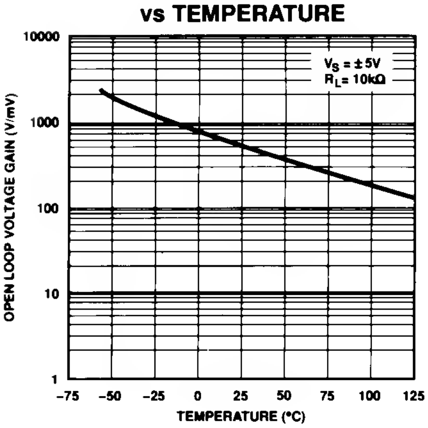
POWER SUPPLY REJECTION vs FREQUENCY



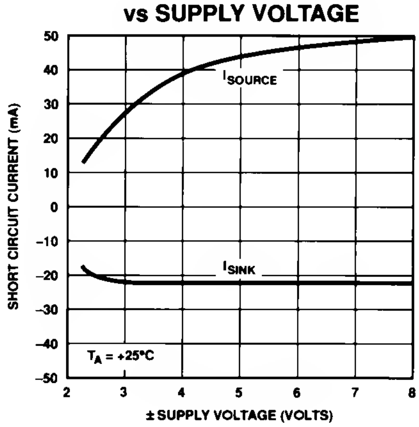
OPEN-LOOP GAIN AND PHASE SHIFT vs FREQUENCY



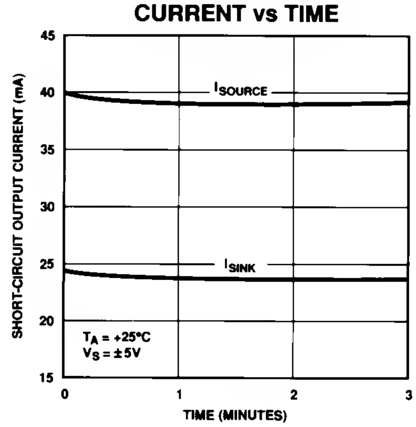
OPEN LOOP GAIN vs TEMPERATURE



SHORT CIRCUIT CURRENT vs SUPPLY VOLTAGE

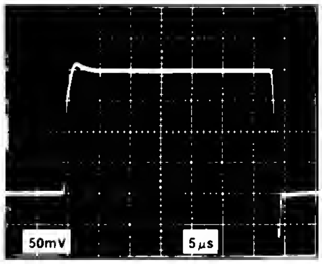


SHORT-CIRCUIT OUTPUT CURRENT vs TIME



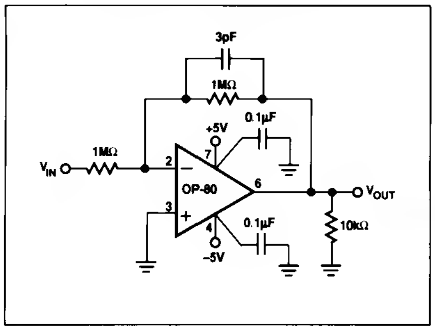
TYPICAL ELECTRICAL CHARACTERISTICS *Continued*

SMALL-SIGNAL TRANSIENT RESPONSE

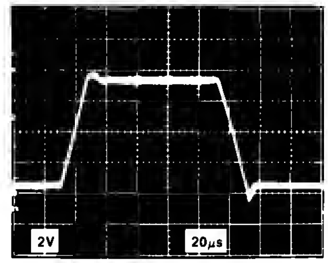


T_A = +25°C
V_S = ±5V
R_L = 10kΩ
C_L = 100pF
A_V = +1

TEST CIRCUIT FOR LARGE-SIGNAL TRANSIENT RESPONSE



LARGE-SIGNAL TRANSIENT RESPONSE



T_A = +25°C
V_S = ± 5V
R_L = 10kΩ
A_V = −1

APPLICATIONS INFORMATION

Offering one of the lowest input currents of any monolithic operational amplifier, the OP-80 is ideal for use in applications measuring signals from a very high impedance or a very low current source. Operating from a single +5V supply, common-mode input voltages extend to ground with the output swinging to within 200μV of ground. It is a true "single-supply operational amplifier."

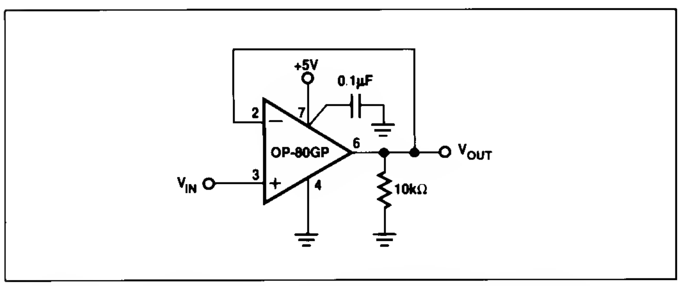


FIGURE 1: *Unity Voltage Gain Follower, Single +5V Supply*

An example of this single-supply operation is illustrated in Figure 1. The OP-80, configured as a unity gain voltage-follower with a single +5V supply, can be operated down to ground, as shown by the 10kHz sinewave output in Figure 2. Typical of CMOS op amp operation, the output stage of the OP-80 requires a output load resistance of 1MΩ or less.

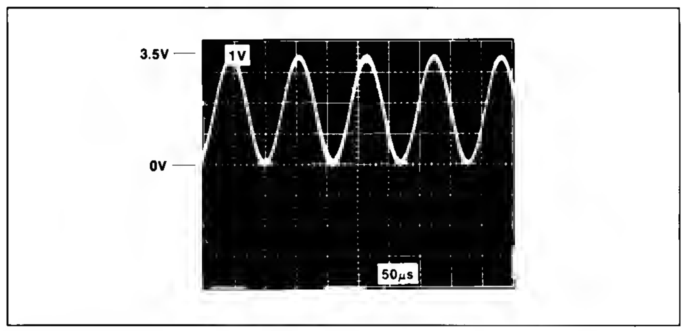


FIGURE 2: *Voltage Follower Response, 10kHz Sine Wave V_S = +5V, R_L = 10kΩ. Note that output extends to ground.*

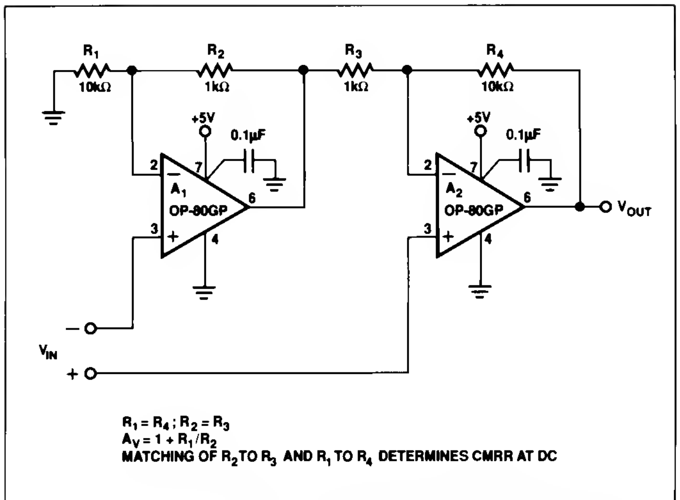


FIGURE 3: *True Single Supply Instrumentation Amplifier*

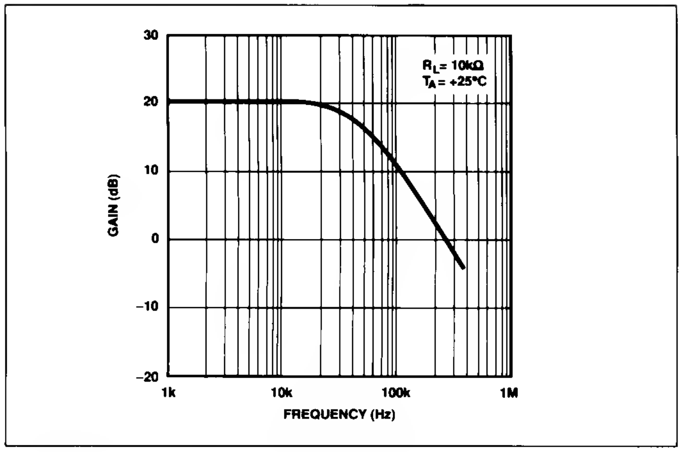


FIGURE 5: *Instrumentation Amplifier Frequency Response*

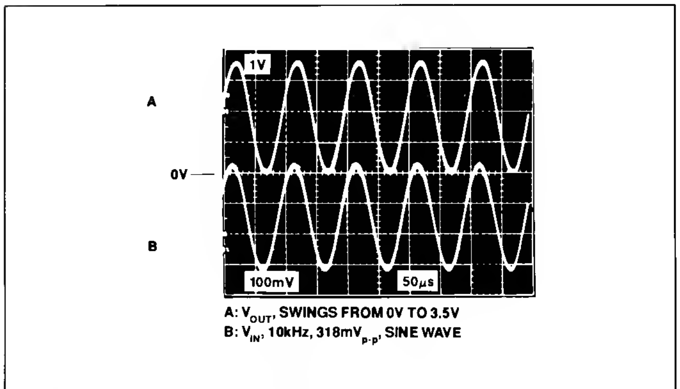


FIGURE 4: *Sine Wave Response*

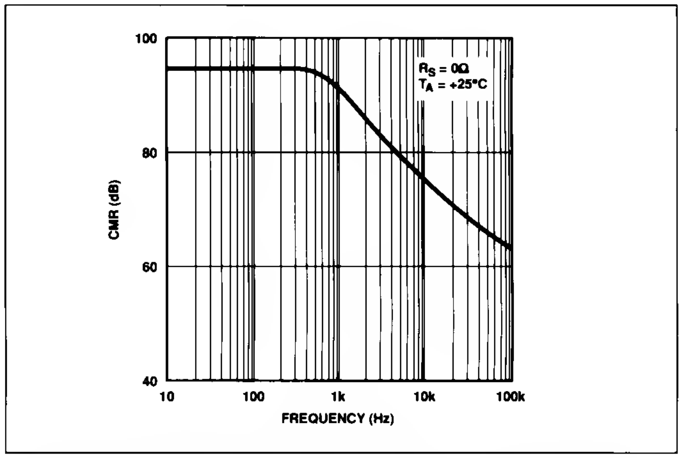


FIGURE 6: *Instrumentation Amplifier Common-Mode Rejection*

A TRUE SINGLE SUPPLY INSTRUMENTATION AMPLIFIER

The circuit in Figure 3 shows an instrumentation amplifier operated from a single +5V supply. This amplifier is quite useful for battery-powered instrument applications since it consumes a supply current of less than 400µA, and the output signal can swing down to ground level, as illustrated in Figure 4.

Although this amplifier topology is not symmetrically balanced, as in a three op-amp instrumentation amplifier, a common-mode rejection of 70dB is still maintained over a signal bandwidth of 20kHz as shown in Figures 5 and 6. Finite open-loop gain of A_1 causes feedthrough of the common-mode input which may be improved by trimming R_1.

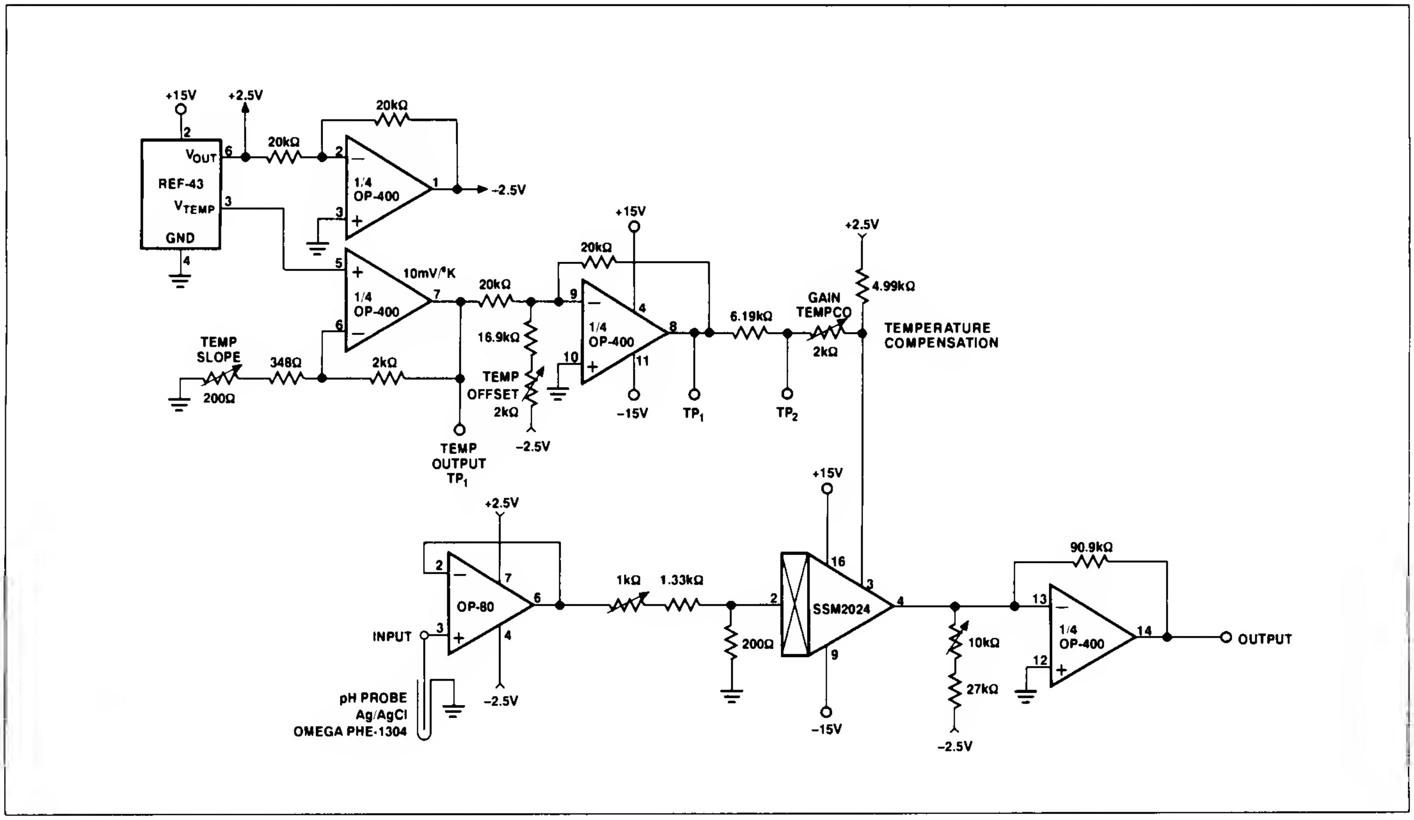


FIGURE 7: *A Complete, Temperature-Compensated pH Meter Design*

IDEAL FOR A pH METER

Since the OP-80 has an extremely high input impedance, it is ideal for pH/Ion sensitive electrode applications. Figure 7 illustrates an OP-80 used to buffer the extremely high impedance of a pH probe. The meter includes a temperature compensation circuit for the probe.

pH Meter Calibration Procedure

1. With T_A = +25°C adjust temperature slope for 2.98V temperature output.
2. Adjust temperature offset @ 25°C for −0.25V at TP_1.
3. Short TP_2 to ground.
4. Apply 0V to input (with pH probe disconnected).
5. Adjust offset for 7V output.
6. Apply +271mV to input; adjust gain trim for 2V output.
7. For improved accuracy, repeat steps 4, 5 and 6 as these adjustments are interactive.
8. Remove ground short from TP_2.
9. With T_A = +25°C, apply +295.6mV to input; adjust gain tempco for 2V output. For highest accuracy, use a buffer solution at a known pH and temperature and set gain tempco for proper output. Remember, to properly set the temperature calibration, the REF-43 must be placed in thermal contact with the solution under test.

The output voltage of the pH probe is linearly dependent on the pH of the sample solution and the sample temperature. A current-controlled amplifier, the SSM2024, is driven by a temperature dependent signal to account for the change in the pH probe's output voltage due to sample temperature variations.

After the pH meter is calibrated, it will have an output of 1V/pH from 2 ≤ pH ≤ 12 and is accurate to 0.01pH at 25°C and 0.05pH from 0°C to 70°C.

The REF-43's V_{TEMP} output provides an output voltage proportional to a temperature, typically 1.9mV/°C. This temperature dependent signal is conditioned and used to provide the correction signal to the current controlled amplifier.

GUARDING AND SHIELDING

To maintain the extremely high input impedances of the OP-80, care must be taken in circuit board layout and manufacturing. Board surfaces must be kept scrupulously clean and free of moisture. Conformal coating is recommended to provide a humidity barrier. Even a clean PC board can have 100pA of leakage currents between adjacent traces where a potential difference is present, so that guard rings should be used around the inputs. Guard traces should be driven at a voltage equal to or close to that of the inputs, so that leakage currents are kept at a minimum. In noninverting applications, the guard ring should be connected to the common-mode voltage at the inverting input (pin 2).

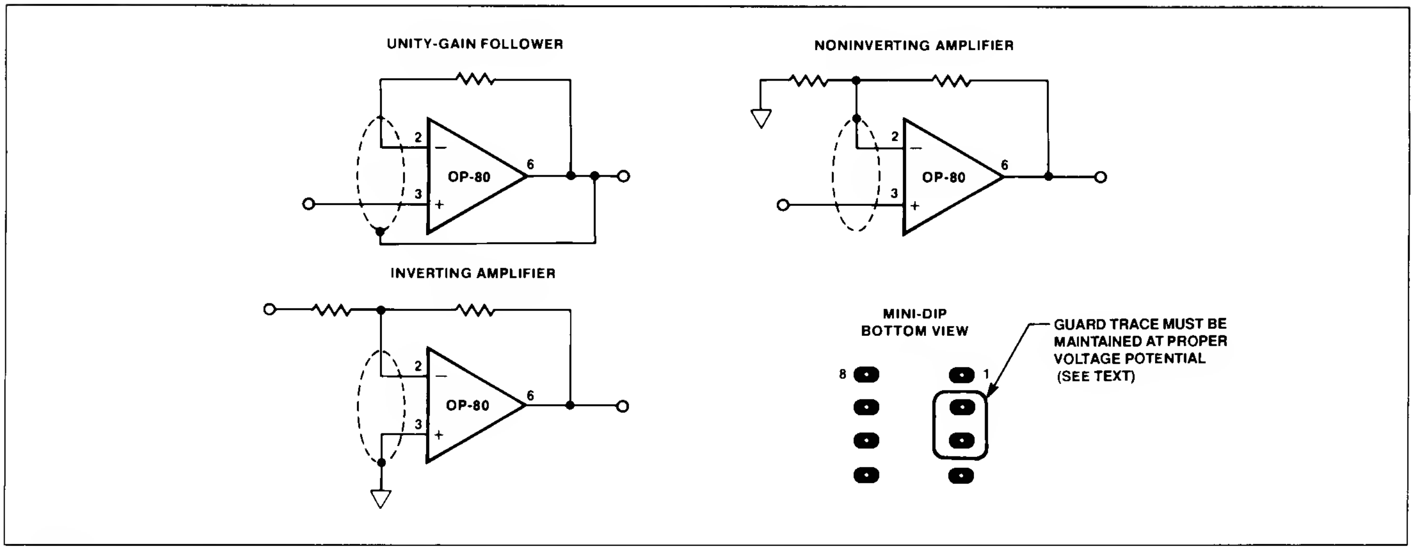


FIGURE 8: *Guard Ring Layout and Connections*

When the OP-80 is operated in the inverting mode, as in Figure 9, the signal traces should have grounded guard traces on both sides of the PC board since both inputs remain at ground voltage potential.

High impedance circuitry is extremely susceptible to RF pickup, line-frequency hum, and radiated noise from switching power-supplies. Enclosing sensitive analog sections within grounded shields is generally necessary to prevent excessive noise pickup. Twisted-pair cable will aid in rejection of line-frequency hum.

The OP-80's AC characteristics are highly stable over a wide range of operating conditions. Due to the extemely high input impedance, the OP-80 can be used with large source impedances, such as I-V converter applications. Input capacitance, with high source impedances, can substantially degrade signal bandwidth and stability margins. Accordingly, guarding the input lines will not only reduce parasitic leakage, but stray capacitance at the input node will also be minimized.

To cancel the effect of the input capacitance, the pole created must be neutralized by a zero that is located at the same frequency. To introduce this zero, place a capacitor, C_F, around the feedback resistor with a value such that:

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_F}$$

or $R_1 C_{IN} \leq R_2 C_F$.

R_1 is modelled as a Thevenin equivalent impedance for I-V converter applications.

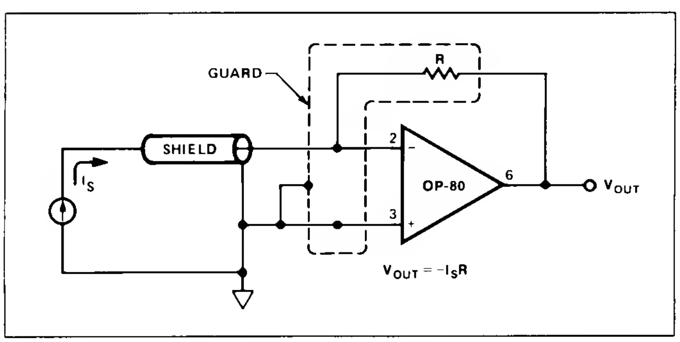


FIGURE 9: *Current-to-Voltage Converter*

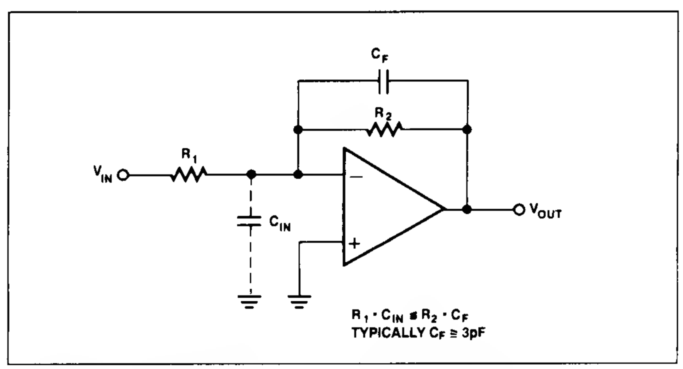


FIGURE 10: *Cancelling the Effect of Input Capacitance*